IN THE CLAIMS:

Claims 3 through 6 are cancelled herein. Claims 1, 7, 8 and 14 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently amended) A method of forming a semiconductor device package, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, the active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of the plurality of individual die locations;

forming intermediate conductive elements over the plurality of bond pads to project a height above the active surface;

forming a pattern of mutually transverse channels in the active surface to a depth below the at least one layer of integrated circuitry, the mutually transverse channels circumscribing a semiconductor device location comprised of at least one individual die and exposing peripheral edges of the at least one layer of integrated circuitry;

applying an encapsulant material at least over the active surface and into the mutually transverse channels to a depth exceeding the height of projection of the intermediate conductive elements;

removing a depth of the encapsulant material sufficient to expose a portion of each of the intermediate conductive elements; and

placing the semiconductor substrate with the intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and

electrically connecting the intermediate conductive elements and the conductive bumps.

2. (Currently Amended) The method of claim 1, further including forming bond pads over the exposed portions of the intermediate conductive elements before electrically connecting the intermediate conductive elements to the conductive bumps.

3.-6. (Cancelled)

7. (Currently amended) The method of claim 1, further comprising forming the mutually transverse channels with sloped side walls defining opposing chamfers.

8. (Currently amended) The method of claim 1, further comprising forming the mutually transverse channels with substantially parallel side walls.

9. (Previously presented) The method of claim 1, wherein forming the intermediate conductive elements is effected by forming at least one solder ball.

10. (Previously presented) The method of claim 1, wherein forming the intermediate conductive elements is effected by forming at least one pillar of a conductive or conductor-filled epoxy or a metal-filled elastomer.

11. (Previously presented) The method of claim 1, wherein forming the intermediate conductive elements is effected by a wire bonding capillary.

12. (Previously presented) The method of claim 1, wherein applying an encapsulant material comprises applying an encapsulant material of a material selected from the group comprising filled polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes and glasses.

13. (Previously presented) The method of claim 1, further comprising applying another layer of encapsulant material on a back side of the semiconductor substrate.

14. (Currently amended) The method of claim 1, further comprising severing the semiconductor substrate along the pattern of mutually transverse channels into a plurality of semiconductor elements, each semiconductor element of the plurality comprised of at least one individual die location.